CLAIMS

What is claimed is:

1. A multi-layer semiconductor chip package, comprising:

a first pair of conductors for carrying a first signal in a layer of a carrier of the package; and

a second pair of conductors for carrying a second signal adjacent to the first pair of conductors in the layer, wherein the first and second pairs of conductors are configured such that cross-talk between the first and second pairs of conductors is substantially minimized without increasing a size of the package.

2. The package of claim 1, wherein a height of the first pair of conductors is substantially shorter than a height of the second pair of conductors.

3. The package of claim 2, wherein the height of the second pair of conductors in a subsequent layer of the carrier is substantially shorter than the height of the first pair of conductors in the subsequent layer.

4. The package of claim 1, wherein the first and second pairs of conductors are positioned so that they affect each other evenly.

5. The package of claim 4, wherein the first and second pairs of conductors are positioned orthogonally to each other.

6. The package of claim 4, wherein the second pair of conductors is positioned to be equidistant to each conductor in the first pair of conductors.

7. The package of claim 1, wherein the layer is near an interface between the carrier and a chip.

8. A multi-layer semiconductor chip package, comprising:

a first pair of conductors for carrying a first signal in a layer of a carrier of the package; and

a second pair of conductors for carrying a second signal adjacent to the first pair of conductors in the layer, wherein a height of the first pair of conductors is substantially shorter than a height of the second pair of conductors such that cross-talk between the first and second pairs of conductors is substantially minimized without increasing a size of the package.

9. The package of claim 8, wherein the height of the second pair of conductors in a subsequent layer of the carrier is shorter than the height of the first pair of conductors in the subsequent layer.

10. The package of claim 8, wherein the layer is near an interface between the carrier and a chip.

11. A multi-layer semiconductor chip package, comprising:

a first pair of conductors for carrying a first signal in a layer of a carrier of the package; and

a second pair of conductors for carrying a second signal adjacent to the first pair of conductors in the layer, wherein the first and second pairs of conductors are positioned so that they affect each other evenly such that cross-talk between the first and second pairs of conductors is substantially minimized without increasing a size of the package.

12. The package of claim 11, wherein the second pair of conductors is positioned to be equidistant to each conductor in the first pair of conductors.

13. The package of claim 11, wherein the first and second pairs of conductors are positioned orthogonally to each other.

14. The package of claim 11, wherein the layer is near an interface between the carrier and a chip.

15. A connector capable of being coupled to a semiconductor chip package, comprising:

a first pair of conductors for carrying a first signal; and

a second pair of conductors for carrying a second signal adjacent to the first pair of conductors, wherein the first and second pairs of conductors are configured such that cross-talk between the first and second pairs of conductors is substantially minimized without increasing a size of the package.

16. The connector of claim 15, wherein the first and second pairs of conductors are positioned so that they affect each other evenly.

17. The connector of claim 16, wherein the second pair of conductors is positioned to be equidistant to each conductor in the first pair of conductors.

18. A method for providing a semiconductor chip package, comprising the steps of:

(a) providing a first pair of conductors for carrying a first signal in a layer of a carrier of the package; and

(b) providing a second pair of conductors for carrying a second signal adjacent to the first pair of conductors in the layer, wherein the first and second pairs of conductors are configured such that cross-talk between the first and second pairs of conductors is substantially minimized without increasing a size of the package.

19. The method of claim 18, wherein the first pair of conductors is provided with a height shorter than a height of the second pair of conductors.

20. The method of claim 19, further comprising:

(c) providing the first and second pairs of conductors in a subsequent layer of the carrier, wherein the height of the second pair of conductors in the subsequent layer is substantially shorter than the height of the first pair of conductors in the subsequent layer.

21. The method of claim 18, wherein the first and second pairs of conductors are positioned so that they affect each other evenly.

22. The method of claim 21, wherein the first and second pairs of conductors and positioned orthogonally to each other.

23. The method of claim 21, wherein the second pair of conductors is positioned to be equidistant to each conductor in the first pair of conductors.

24. The method of claim 18, wherein the layer is near an interface between the carrier and a chip.